FEATURES

- 2688 x 512 CCD Image Array
- 15 μm x 15 μm Pixel
- 40.32mm x 7.68mm Image Area
- 100% Fill Factor
- Readout Noise Less Than 3 Electrons at 50KHz
- 2 Single Stage 500kHz Outputs
- Three-Phase Buried Channel Image area
- Three-Phase Buried Channel Serial Readout Registers

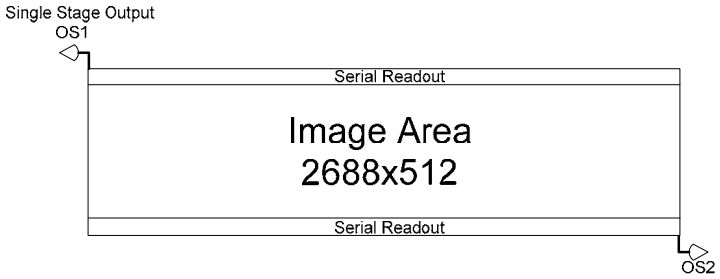

Fig. 1 STA0520A Block Diagram

GENERAL DESCRIPTION

The STA0520A is a 2688 x 512 pixel solid state Charge Coupled Device CCD sensor. This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems. The STA0520A is a single array of 2688 horizontal by 512 vertical photosites. The pixel spacing is 15μm x 15μm. An implant under A3 makes possible Multi-Pinned Phase operation for reduced dark current at any give temperature.

FUNCTIONAL DESCRIPTION

The following functional elements are illustrated in the block diagram:

Image Charge Shifting:

The imaging area is a full 2688 x 512. A 3 phase serial readout register along the top and bottom permits multiple readout modes of the array.

Integration:

During integration A1U/A1L are held high and A2U/A2L, A3U/A3L are held low.

Full Frame Mode:

A complete image can be readout either serial register by tying together A1U+A1L, A2U+A2L, and A3U+A3L, see Fig. 4. For simplicity one should tie ATGL to A2L and ATGU to A3U.

To each serial register individually both the horizontal and vertical directions depending on the, configuration of the A1, A2, A3 clocks. For normal vertical CCD readout the charge is clocked up and out in A1-A2-A3 order.

Parallel phase A1 is the final array gate before charge is transferred to the serial horizontal shift register.

Serial Charge Readout: S1,S2 and S3 are polysilicon gates used to transfer charge horizontally to the output amplifiers. The serial transport register is twice the size of the pixel to allow for vertical binning.

Each serial register has 16 additional register cells between the column of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference

The last clocked gate SW in the serial register can be clocked separately or tied to S3 for normal operation.

The output sense node is reset with RG.

Output Amplifier: The STA1050A has two single stage output amplifiers at the end of each serial register, see schematic. T

The output amplifier drain is tied to VD. The source is connected to an external load resistor to ground, typically 10k.

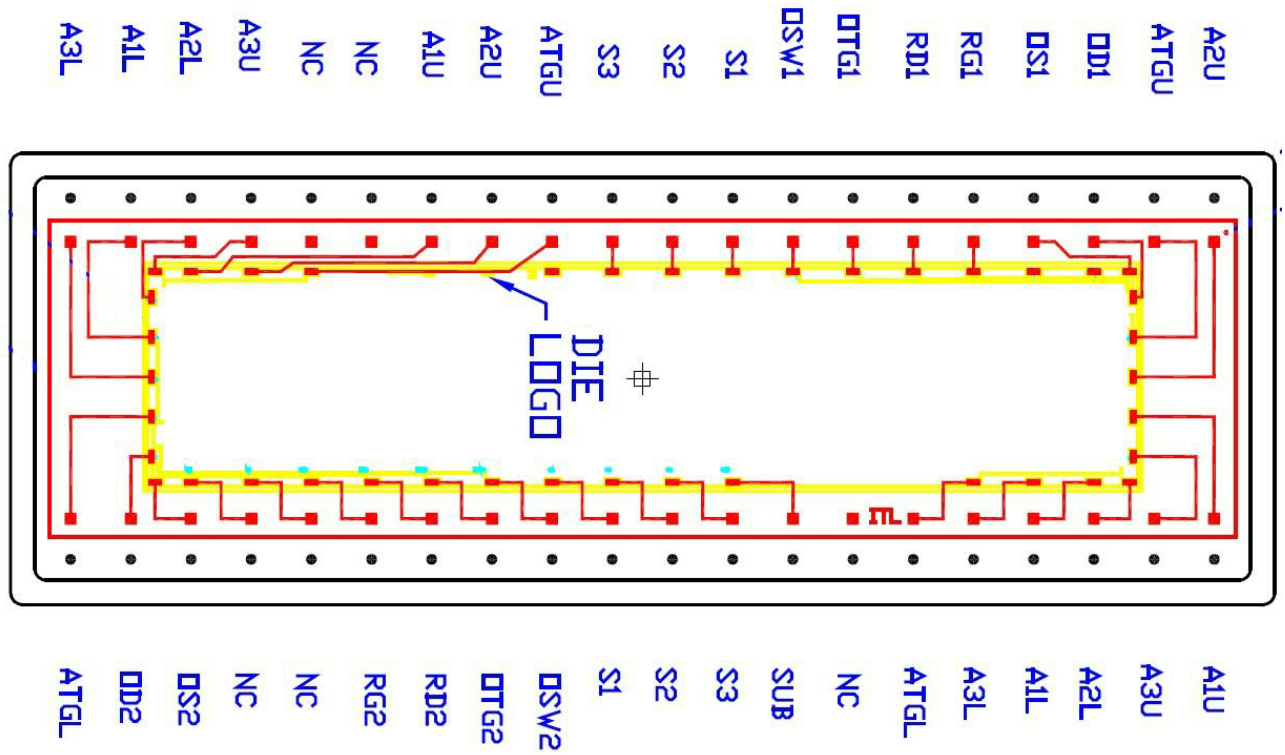

Fig. 2 STA0520A Backside Illuminated Package Pinout

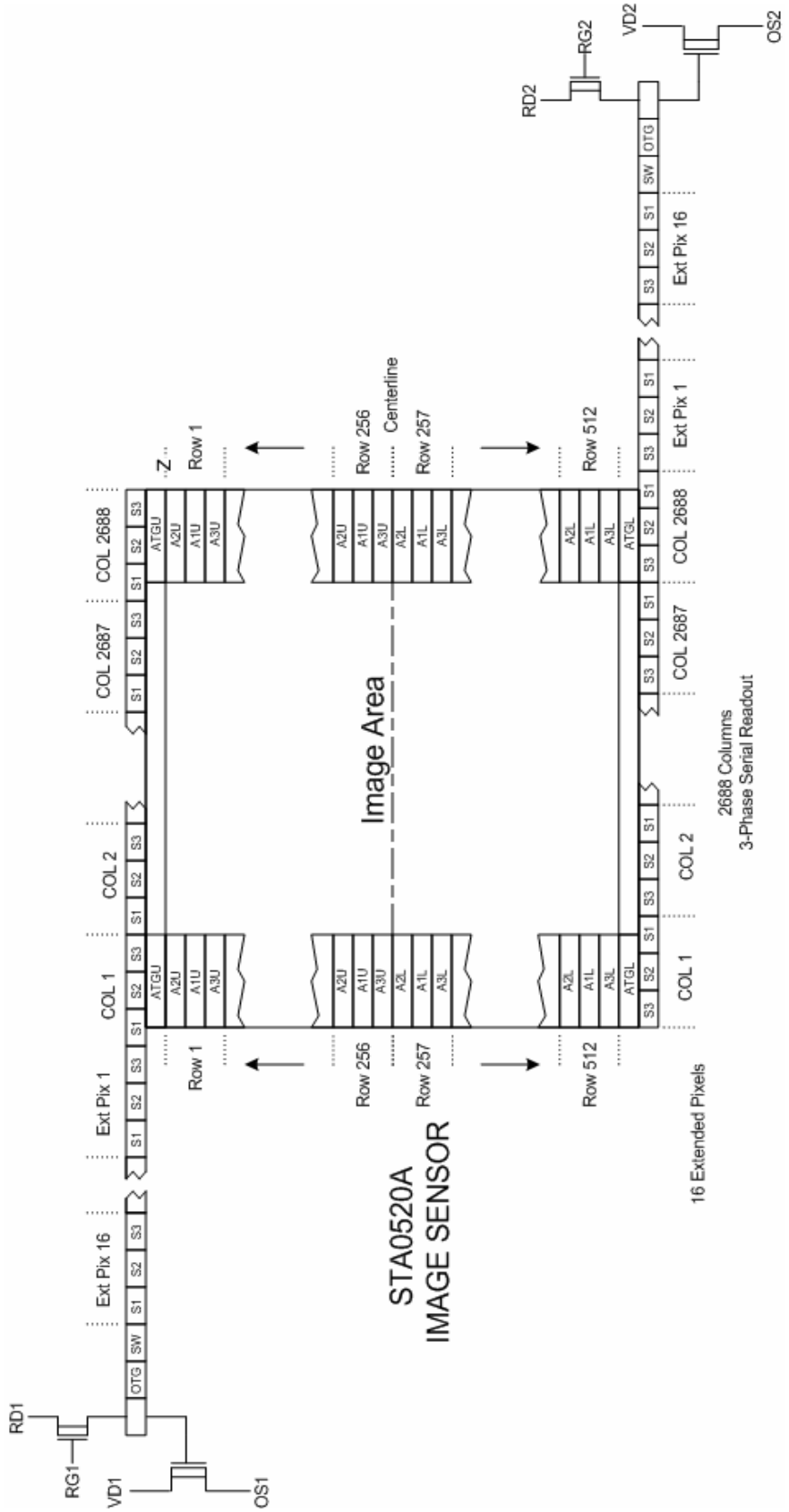

Fig. 3 STA0520A Device Schematic

DC OPERATING CHARACTERISTICS						
SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
VD	DC Supply Voltage	15.0	24.0	30.0	V	
RD	Reset Drain Voltage	10.0	15.0	20.0	V	
OTG	Output Transfer Gate Voltage	-2.0	-1.0	2.0	V	
Vss	Substrate Ground		0.0		V	
TYPICAL CLOCK VOLTAGES						
SYMBOL	PARAMETER	HIGH		LOW	UNIT	REMARKS
S1,S2,S3	Horizontal Serial Clocks	+5.0		-5.0	V	Typical clock range
SW	Summing Gate Clock	+5.0		-5.0	V	Clock as S3 if not clocked separately
A1,A2,A3,ATGU, ATGL	Vertical Array Clocks	+4.0		-9.0	V	
Rg	Reset Gate Array Clock	+8.0		-0.0	V	
AC CHARACTERISTICS						
SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
V_{ODC}	Output DC Level		14.0		V	Typical
Z	Suggested Load Resistor	5.0	10.0	20.0	kΩ	
PERFORMANCE SPECIFICATIONS						
SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
V_{SAT}	Saturation Output Voltage Full Well Capacity		600 150k		mV e-	
	Output amplifier sensitivity		5.0		μV/e-	
PRNU	Photo Response Non-Uniformity Peak-to-Peak		10		$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak		1.0		mV	

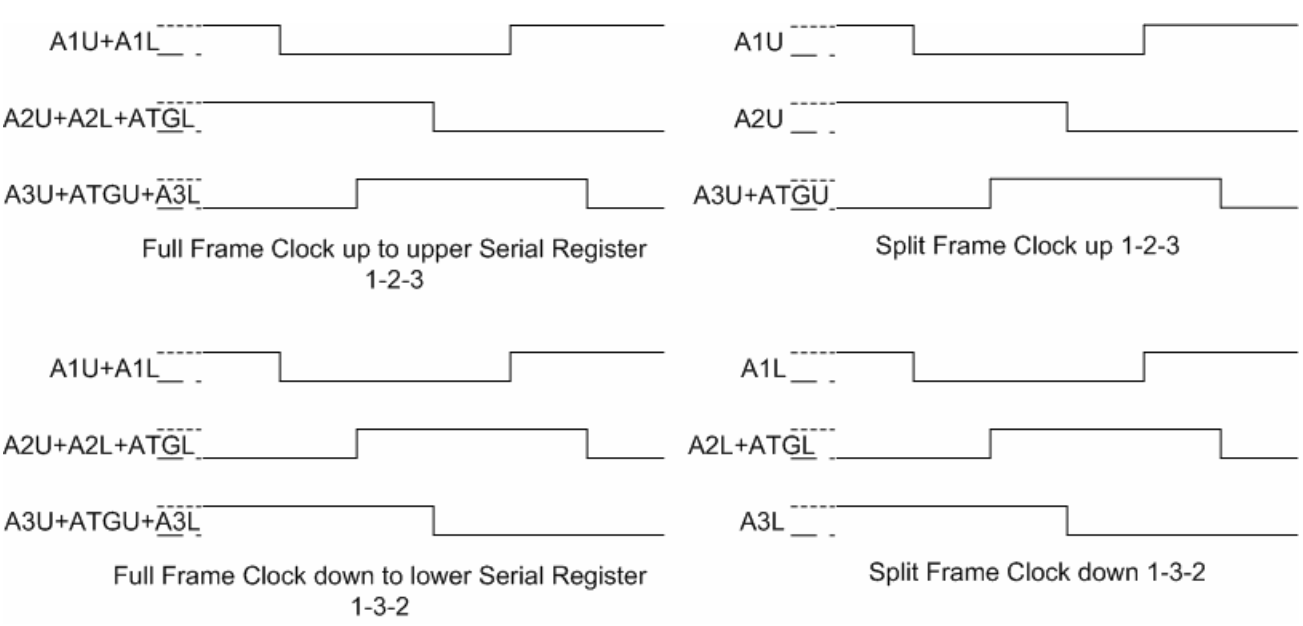

Fig. 4 Vertical Clock Timing for various modes

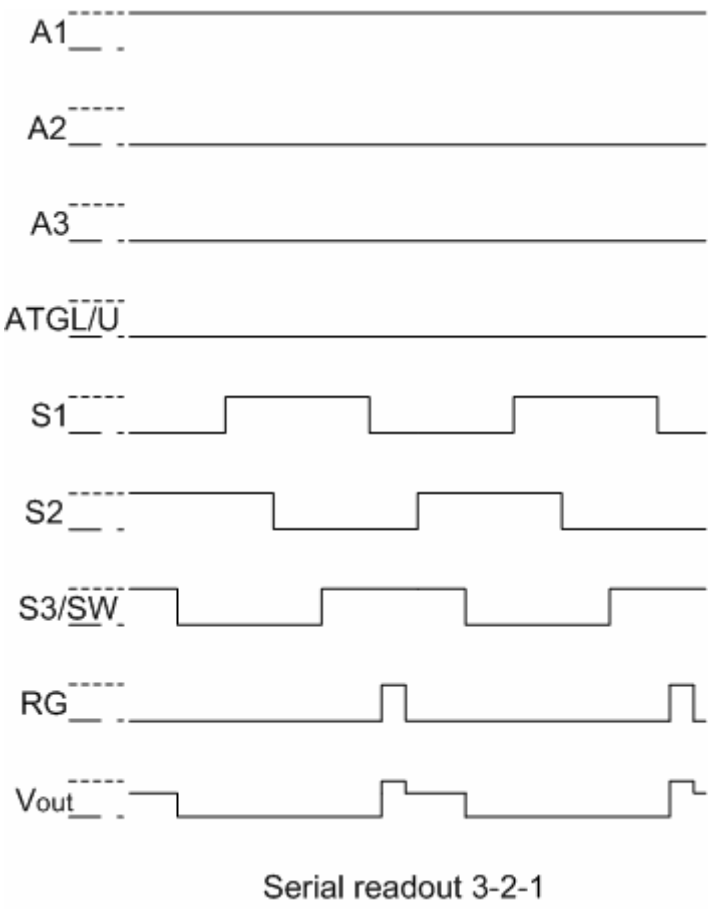

Fig. 5 Normal Serial Clock timing